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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,021	07/26/2001	Chien-Ping Huang	71987-10000	8130

7590 12/31/2002
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EXAMINER

CHU, CHRIS C

ART UNIT PAPER NUMBER

2815

DATE MAILED: 12/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/916,021	Applicant(s) HUANG ET AL.	
	Examiner Chris C. Chu	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 15 October 2002.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1 - 20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1 - 20 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 26 July 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some * c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6) <input type="checkbox"/> Other:
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DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on October 15, 2002 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following limitation in claims 1 and 12 "an encapsulant made of the molding compound for encapsulating the chip, the buffer pad, the heat sink and the chip carrier" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Claim Objections

4. Claim 1 is objected to because of the following informalities: in line 8 form bottom, "heat sink" should be --the heat sink--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1 ~ 4, 6, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Morishita et al.

Regarding claim 1, Johnson et al. discloses in Figs. 15 and 16 a semiconductor package with a heat sink, comprising:

- a chip carrier (12);
- at least one chip (14) mounted on the chip carrier (12) and electrically connected to the chip carrier (see Figs. 15 and 16);
- a heat sink (40) having a first surface, a second surface opposed to the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface (see Figs. 15 and 16), wherein the first surface of the heat sink is attached to

the chip for interposing the chip between the chip carrier and the heat sink (see Figs. 15 and 16);

- an interface layer (41, the top) formed on the second surface of the heat sink; and
- an encapsulant (24) made of the molding compound for encapsulating the chip, heat sink and the chip carrier, wherein the interface layer (41, the top) and the side surfaces of the heat sink (40) are exposed to outside of the encapsulant (see Figs. 15 and 16), and the side surfaces of the heat sink (40) are flush with side edges of the encapsulant (24 and see Figs. 15 and 16).

Johnson et al. does not disclose a material of an interface layer and a size of the interface layer to cover the entire second surface of the heat sink. However, Morishita et al. discloses in Fig. 2 and column 3, line 4 an interface layer (12) formed on the second surface of the heat sink (10), and made of a material having adhesion with a molding compound smaller than adhesion between a heat sink and a molding compound, wherein the interface layer covers the entire second surface of the heat sink. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Johnson et al. by using the material of an interface layer and the size of the interface layer to be covering the entire second surface of the heat sink as taught by Morishita et al. The ordinary artisan would have been motivated to modify Johnson et al. in the manner described above for at least the purpose of preventing electrolytic corrosion (column 3, lines 51 ~ 53). Further, the limitation “whereby due to relatively smaller adhesion between the interface layer and the molding compound for making the encapsulant, the molding compound remaining on the interface layer during formation of the encapsulant can be removed easily from the interface layer, so as to make the semiconductor package free of flash of

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the molding compound” has been held that the functional “whereby” statement does not define any structure and accordingly can not serve to distinguish. In re Mason, 114 USPQ 127, 44 CCPA 937 (1957).

Regarding claim 2, Johnson et al. discloses in Figs. 15 and 16 the heat sink having a surface area dimensionally same as that of the chip carrier.

Regarding claim 3, Morishita et al. discloses in Fig. 2 and column 3, line 4 the material for making the interface layer on the second surface of the heat sink being nickel.

Regarding claim 4, Johnson et al. discloses in Fig. 15, Fig. 16 and column 3, line 29 the chip carrier being a substrate.

Regarding claim 6, Johnson et al. discloses in Fig. 15, Fig. 16 the chip being electrically connected to the substrate through solder bumps.

Regarding claim 9, since Johnson et al. does not disclose grinding the surface of the heat sink, the surface thereof is inherently roughened, corrugated or made uneven.

Regarding claim 10, Johnson et al. discloses in Fig. 15, Fig. 16 at a position on the first surface of the heat sink corresponding to the chip (14) there is formed a connecting portion (41, the bottom) extending toward the chip (14) for connecting the heat sink (40) to the chip (14) through the connecting portion (see Fig. 16), and the first surface of the heat sink (40) other than the position of the connecting portion being spaced apart from the chip (see Fig. 16).

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. and Morishita et al. as applied to claims 1 and 4 above, and further in view of DiStefano.

Johnson et al. and Morishita et al. disclose the claimed invention except for the chip being electrically connected to the substrate through bonding wires. However, DiStefano discloses in Fig. 4 and column 7, lines 44 ~ 46 a chip being electrically connected to a substrate through bonding wires (156). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Johnson et al. by using the bonding wires as taught by DiStefano. The ordinary artisan would have been motivated to further modify Johnson et al. in the manner described above for at least the purpose of reducing heat between chip and substrate.

8. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. and Morishita et al. as applied to claim 1 above, and further in view of Huang et al.

Johnson et al. and Morishita et al. disclose the claimed invention except for the chip carrier being a QFN (quad flat nonlead) lead frame and wherein the chip being electrically connected to the QFN lead frame through bonding wires. However, Huang et al. discloses in Figs. 1 ~ 7 and column 3, lines 30 ~ 31 a chip carrier being a QFN (quad flat nonlead) lead frame and wherein the chip being electrically connected to the QFN lead frame through bonding wires (216 in Fig. 6 and 316 in Fig. 7). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Johnson et al. by using the QFN (quad flat nonlead) lead frame and the bonding wires as taught by Huang et al. The ordinary artisan would have been motivated to further modify Johnson et al. in the manner described above for at least the purpose of improving the heat-dissipating effect of the package (column 2, lines 8 ~ 10).

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. and Morishita et al. as applied to claim 1 above, and further in view of Karnezos.

Regarding claim 11, a further difference between Johnson et al. in view of Morishita et al. and claimed invention is wherein the heat sink is attached to the chip through a thermally conductive adhesive. However, Karnezos discloses in Fig. 3A and read column 7, lines 61 ~ 65 a heat sink being attached to a chip through a thermally conductive adhesive (113). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Johnson et al. by using the thermally conductive adhesive as taught by Karnezos. The ordinary artisan would have been motivated to further modify Johnson et al. in the manner described above for at least the purpose of increasing bond strength between the heat sink and the chip.

10. Claims 12 ~16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Morishita et al., and further in view of Lai et al.

Regarding claim 12, Johnson et al. discloses in Figs. 15 and 16 a semiconductor package with a heat sink, comprising:

- a chip carrier (12);
- at least one chip (14) mounted on the chip carrier (12) and electrically connected to the chip carrier (see Figs. 15 and 16);
- a heat sink (40) having a first surface, a second surface opposed to the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface (see Figs. 15 and 16);

- an interface layer (41, the top) formed on the second surface of the heat sink; and
- an encapsulant (24) made of the molding compound for encapsulating the chip, the buffer pad, the heat sink and the chip carrier, wherein the interface layer (41, the top) and the side surfaces of the heat sink (40) are exposed to outside of the encapsulant (see Figs. 15 and 16), and the side surfaces of the heat sink (40) are flush with side edges of the encapsulant (24 and see Figs. 15 and 16).

Johnson et al. does not disclose a material of an interface layer and a size of the interface layer to cover the entire second surface of the heat sink. However, Morishita et al. discloses in Fig. 2 and column 3, line 4 an interface layer (12) formed on the second surface of the heat sink (10), and made of a material having adhesion with a molding compound smaller than adhesion between a heat sink and a molding compound, wherein the interface layer covers the entire second surface of the heat sink. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Johnson et al. by using the material of an interface layer and the size of the interface layer to be covering the entire second surface of the heat sink as taught by Morishita et al. The ordinary artisan would have been motivated to modify Johnson et al. in the manner described above for at least the purpose of preventing electrolytic corrosion (column 3, lines 51 ~ 53).

Further, a further difference between Johnson et al. in view of Morishita et al. and claimed invention is at least one buffer pad attached to the chip and made of a material having a similar thermal expansion coefficient to the chip and a location of the buffer pad. However, Lai et al. discloses in Fig. 2 and column 4, lines 52 ~ 67 at least one buffer pad (5) attached to the chip (3) and made of a material having a similar thermal expansion coefficient to the chip and

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the first surface of a heat sink (4) being attached to the buffer pad (5) for interposing the buffer pad between the heat sink and a chip (3) so as to space the first surface apart from the chip. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Johnson et al. by using the buffer pad as taught by Lai et al. The ordinary artisan would have been motivated to further modify Johnson et al. in the manner described above for at least the purpose of preventing thermal compressive stress and tensile stress resulted from the encapsulant during packaging process (column 3, lines 1 ~ 7). Furthermore, the limitation “whereby due to relatively smaller adhesion between the interface layer and the molding compound for making the encapsulant, the molding compound remaining on the interface layer during formation of the encapsulant can be removed easily from the interface layer, so as to make the semiconductor package free of flash of the molding compound” has been held that the functional “whereby” statement does not define any structure and accordingly can not serve to distinguish. In re Mason, 114 USPQ 127, 44 CCPA 937 (1957).

Further, Johnson et al. discloses the limitation “wherein adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound” since there is no encapsulant material contacting the interface layer (41, the top).

Regarding claim 13, Johnson et al. discloses in Figs. 15 and 16 the heat sink having a surface area dimensionally same as that of the chip carrier.

Regarding claim 14, Morishita et al. discloses in Fig. 2 and column 3, line 4 the material for making the interface layer on the second surface of the heat sink being nickel.

Regarding claim 15, Johnson et al. discloses in Fig. 15, Fig. 16 and column 3, line 29 the chip carrier being a substrate.

Regarding claims 16 and 20, a further difference between Johnson et al. in view of Morishita et al. and claimed invention is wherein the chip is electrically connected to the substrate through bonding wires and wherein the heat sink is attached to the buffer pad through a thermally conductive adhesive. However, Lai et al. discloses in Fig. 2, Fig. 3, column 5, lines 6 ~ 9 and column 6, lines 50 ~ 56 a chip (3) being electrically connected to a substrate (2) through bonding wires (8) and wherein a heat sink (4a) being attached to a buffer pad (5a) through a thermally conductive adhesive (6a). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Johnson et al. by using the bonding wires and the thermally conductive adhesive as taught by Lai et al. The ordinary artisan would have been motivated to further modify Johnson et al. in the manner described above for at least the purpose of preventing thermal compressive stress and tensile stress resulted from the encapsulant during packaging process (column 6, lines 53 ~ 56).

Regarding claim 19, since Johnson et al. does not disclose grinding the surface of the heat sink, the surface thereof is inherently roughened, corrugated or made uneven.

11. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al., Morishita et al. and Lai et al. as applied to claim 12 above, and further in view of Huang et al.

Johnson et al., as modified, discloses the claimed invention except for the chip carrier is a QFN (quad flat nonlead) lead frame and wherein the chip is electrically connected to the QFN lead frame through bonding wires. However, Huang et al. discloses in Figs. 1 ~ 7 and column 3, lines 30 ~ 31 a chip carrier being a QFN (quad flat nonlead) lead frame and wherein the chip

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being electrically connected to the QFN lead frame through bonding wires (216 in Fig. 6 and 316 in Fig. 7). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Johnson et al. by using the QFN (quad flat nonlead) lead frame and the bonding wires as taught by Huang et al. The ordinary artisan would have been motivated to further modify Johnson et al. in the manner described above for at least the purpose of improving the heat-dissipating effect of the package (column 2, lines 8 ~ 10).

Response to Arguments

12. Applicant's arguments with respect to claims 1, 3, 10, 12 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the


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organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
December 30, 2002



EDITH LEE
SUPERVISOR
TECHNOLOGY CENTER